What is claimed is:

1. A single electron transistor having a memory function, comprising:

a first substrate;

an insulation film stacked on the first substrate;

a second substrate stacked on the insulation film and including a source region, a channel region, and a drain region;

a tunneling film formed on the second substrate;

at least two trap layers formed on the tunneling film and separated by an interval such that at least one quantum dot can be formed in a same interval in the channel region; and

a gate electrode contacting the at least two trap layers and the tunneling film between the at least two trap layers.

2. The single electron transistor as claimed in claim 1, wherein the gate electrode extends on the at least two trap layers.

3. The single electron transistor as claimed in claim 1, wherein the insulation film and the tunneling film are silicon oxide films.

4. The single electron transistor as claimed in claim 1, wherein a size of the at least one quantum dot is 100 nm or less at room temperature.

5. The single electron transistor as claimed in claim 1, wherein the at least two trap layers are nitride layers or ferro-dielectric layers including PZT layers.

6. A single electron transistor having a memory function, comprising:

a first substrate;

a first insulation film stacked on the first substrate;

a second substrate stacked on the first insulation film and including a source region, a channel region, and a drain region;

a second insulation film formed on the second substrate;

at least two trap layers included in the second insulation film and separated by an interval such that at least one quantum dot can be formed in a same interval in the channel region, wherein electrons passing through the channel region are trapped in the at least two trap layers; and

a gate electrode formed on the second insulation film.

7. The single electron transistor as claimed in claim 6, wherein the at least two trap layers are nitride layers or ferro-dielectric layers.

8. The single electron transistor as claimed in claim 6, wherein the at least two trap layers are completely covered with the second insulation film.

9. The single electron transistor as claimed in claim 8, wherein the at least two trap layers are layers selected from the group consisting of conductive material layers including a conductive silicon layer and a conductive germanium layer.

10. The single electron transistor as claimed in claim 6, wherein both the first and second insulation films are oxide films.

11. The single electron transistor as claimed in claim 6, wherein a size of the at least one quantum dot is 100 nm or less at room temperature.

12. A single electron transistor having a memory function, comprising:

a first substrate;

a first insulation film stacked on the first substrate;

a second substrate stacked on the first insulation film and including a source region, a channel region, and a drain region;

a second insulation film formed on the second substrate;

a trap layer continuously formed on the second insulation film;

a third insulation film formed on the trap layer;

at least two fourth insulation film patterns formed on the third insulation film and having conductive spacers formed on facing ends thereof, wherein the conductive spacers are separated by an interval such that at least one quantum dot can be formed in a same interval in the channel region;

a fifth insulation film formed on and between the at least two fourth insulation film patterns having the conductive spacers formed thereon; and

a gate electrode formed on the fifth insulation film.

13. The single electron transistor as claimed in claim 12, wherein the first, second and third insulation films are silicon oxide films.

14. The single electron transistor as claimed in claim 12, wherein the conductive spacers are silicon spacers.

15. The single electron transistor as claimed in claim 12, wherein a size of the at least one quantum dot is 100 nm or less at room temperature.

16. The single electron transistor as claimed in claim 12, wherein the trap layer is a nitride layer or a ferro-dielectric layer.

17. The single electron transistor as claimed in claim 12, wherein each of the second insulation film, the trap layer and the third insulation film have a same thickness.

18. The single electron transistor as claimed in claim 13, wherein a thickness of the fifth insulation film is greater than a thickness of the second insulation film and a thickness of the third insulation film.

19. A single electron transistor having a memory function, comprising:

a first substrate;

a first insulation film stacked on the first substrate;

a second substrate stacked on the first insulation film and including a source region, a channel region, and a drain region;

a second insulation film formed on the second substrate;

at least two trap layer patterns having a separation distance therebetween formed on the second insulation film and in a third insulation film such that the third insulation film surrounds the at least two trap layer patterns on all surfaces except bottom surfaces thereof which contact the second insulation film;

at least two fourth insulation film patterns formed on the third insulation film and having conductive spacers formed on facing ends thereof, wherein the conductive spacers are formed to be in alignment with the at least two trap layer patterns and to be separated from each other by an interval such that at least one quantum dot can be formed in a same interval in the channel region, wherein the interval corresponds to the separation distance between the at least two trap layer patterns;

a fifth insulation film formed on and between the at least two fourth insulation film patterns having the conductive spacers formed thereon; and

a gate electrode formed on the fifth insulation film.

20. The single electron transistor as claimed in claim 19, wherein the at least two trap layer patterns are formed of a material selected from the group consisting of conductive materials including conductive silicon and conductive germanium.

21. The single electron transistor as claimed in claim 19, wherein the at least two trap layer patterns are formed of nitride or a ferro-dielectric.

22. A single electron transistor having a memory function, comprising:

a first substrate;

a first insulation film stacked on the first substrate;

a second substrate stacked on the first insulation film and including a source region, a channel region, and a drain region;

a second insulation film formed on the second substrate;

a trap layer continuously formed on the second insulation film;

a third insulation film formed on the trap layer;

a lower gate continuously formed on the third insulation film;

a fourth insulation film formed on the lower gate;

at least two upper gates formed on the fourth insulation film to be separated from each other by an interval such that at least one quantum dot can be formed in a same interval in the channel region.

23. The single electron transistor as claimed in claim 22, wherein the first through the fourth insulation films are oxide films.

24. The single electron transistor as claimed in claim 22, wherein the trap layer is a nitride layer or a ferro-dielectric layer.

25. The single electron transistor as claimed in claim 22, wherein the trap layer is a layer selected from the group consisting of conductive material layers including conductive silicon layers and conductive germanium layers.

26. A single electron transistor having a memory function, comprising:

a first substrate;

a first insulation film stacked on the first substrate;

a second substrate stacked on the first insulation film and including a source region, a channel region, and a drain region;

a second insulation film formed on the second substrate;

at least two trap layer patterns having a separation distance therebetween formed on the second insulation film and in a third insulation film such that the third insulation film surrounds the at least two trap layer patterns on all surfaces except bottom surfaces thereof which contact the second insulation film;

a lower gate continuously formed on the third insulation film;

a fourth insulation film formed on the lower gate;

at least two upper gates formed on the fourth insulation film to be aligned with the at least two trap layer patterns, and to be separated from each other by an interval such that at least one quantum dot can be formed in a same interval in the channel region, the interval corresponding to the separation distance between the at least two trap layer patterns.

27. The single electron transistor as claimed in claim 26, wherein the at least two trap layer patterns are formed of a material selected from the group consisting of conductive materials including conductive silicon and conductive germanium.

28. The single electron transistor as claimed in claim 26, wherein the trap layer patterns are formed of nitride or a ferro-dielectric.

29. A method of fabricating a single electron transistor, the method comprising:

sequentially stacking an insulation film and a second semiconductor layer on a first semiconductor layer;

forming a tunneling film on the second semiconductor layer;

forming at least two trap layers on the tunneling film to be separated from each other by an interval such that at least one quantum dot can be formed in a same interval in a predetermined region of the second semiconductor layer;

forming a gate electrode in contact with the tunneling film between the at least two trap layers; and

forming a source region and a drain region in the second semiconductor layer such that the source region and the drain region are separated by an interval that is greater than the interval between the at least two trap layers, wherein the source region and the drain region are each doped with conductive impurities.

30. The method as claimed in claim 29, wherein the gate electrode is further formed on all exposed surfaces of the at least two trap layers.

31. The method as claimed in claim 29, wherein the gate electrode is further formed on a portion of each of the at least two trap layers.

32. The method as claimed in claim 29, wherein forming the gate electrode further comprises:

growing the tunneling film to cover the at least two trap layers; and

forming the gate electrode on the entire surface of the tunneling film grown on the at least two trap layers.

33. The method as claimed in claim 29, wherein forming the gate electrode further comprises:

growing the tunneling film to cover the at least two trap layers; and

forming the gate electrode on a portion of the tunneling film grown on the at least two trap layers.

34. The method as claimed in claim 30, wherein forming the source and the drain regions further comprises:

forming a mask pattern on the gate electrode; and

ion implanting the conductive impurities into a resultant structure on which the mask pattern has been formed.

35. The method as claimed in claim 31, wherein the source and drain regions are formed by ion implanting the conductive impurities into a resultant structure in which the gate electrode has been formed, using the gate electrode as a mask.

36. The method as claimed in claim 32, wherein forming the source and the drain regions further comprises:

forming a mask pattern on the gate electrode; and

ion implanting the conductive impurities into a resultant structure on which the mask pattern has been formed.

37. The method as claimed in claim 33, wherein the source and drain regions are formed by ion implanting the conductive impurities into a resultant structure in which the gate electrode has been formed, using the gate electrode as a mask.

38. The method as claimed in claim 29, wherein the at least two trap layers are formed of a nitride or a ferro-dielectric material, each having a trap density of at least $10^{12}/cm^2$.

39. The method as claimed in claim 32, wherein the tunneling film is grown to completely cover the at least two trap layers.

40. The method as claimed in claim 33, wherein the tunneling film is grown to completely cover the at least two trap layers.

41. The method as claimed in claim 29, wherein the at least two trap layers are formed of one material selected from the group consisting of conductive materials including conductive silicon and conductive germanium.

42. The method as claimed in claim 29, wherein the insulation film and the tunneling film are formed of an oxide film.

43. The method as claimed in claim 29, wherein a size of the quantum dot is 100 nm or less at room temperature.